IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Tabery et al.

Serial No.: 10/816,764

Filed: April 2, 2004

Group Art Unit: 2825

Before the Examiner: Naum B. Levin

Title: SYSTEM AND METHOD FOR INTEGRATED CIRCUIT DEVICE DESIGN AND MANUFACTURE USING OPTICAL RULE CHECKING TO SCREEN RESOLUTION ENHANCEMENT TECHNIQUES

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action having a mailing date of October 18, 2006, having a one-month shortened statutory period for response set to expire on November 18, 2006, the Applicants hereby respond as follows:

The Examiner has required a restriction to one of the following inventions:

I. Claims 1-16, drawn to a method of manufacturing an integrated circuit (IC) device having a given layout by simulating how structures within the layout will pattern on a wafer for a plurality of resolution enhancement techniques (RETs), classified in class 716, subclass 21.

II. Claims 17-21, drawn to a photolithography processing system comprising for each combination of numerical aperture (NA) values, illuminator parameters and reticle parameters, classifying structures within the associated simulated layouts based on manufacturability, classified in class 716, subclass 21.

III. Claims 22-24, drawn to a method of minimizing wafer critical dimension (CD) variation in an integrated circuit (IC) device wafer patterned with a desired layout, classified in class 716, subclass 21.

Applicants elect Group I (claims 1-16) without traverse.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorneys for Applicants

By: _____
Robert A. Voigt, Jr.
Reg. No. 47,159

P.O. Box 50784
Dallas, Texas 75201
(512) 370-2832

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